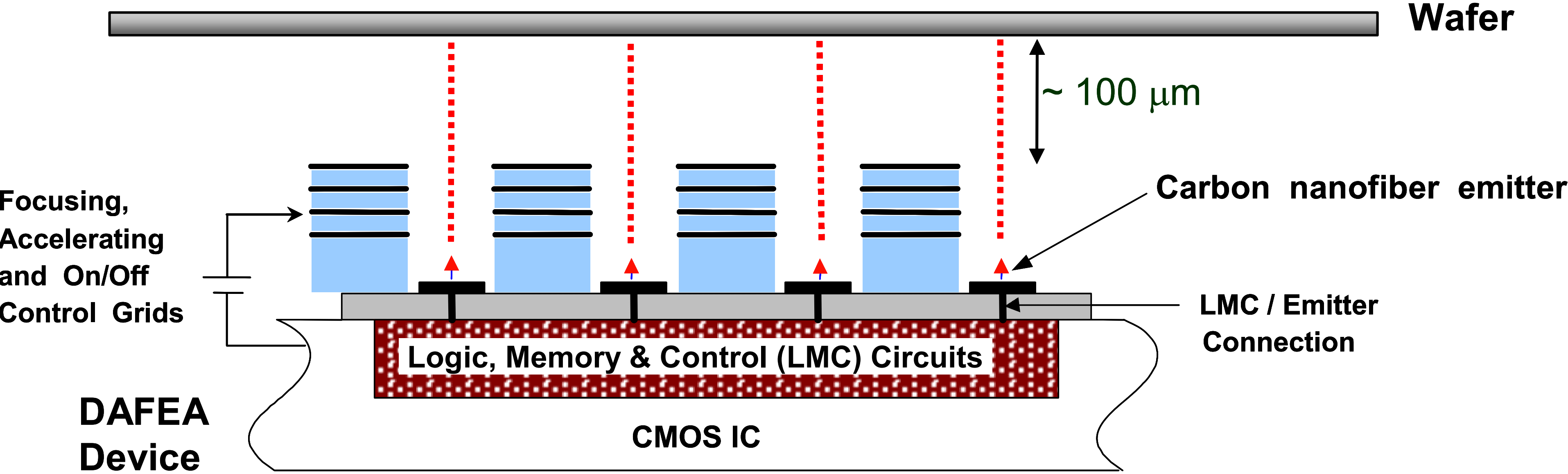
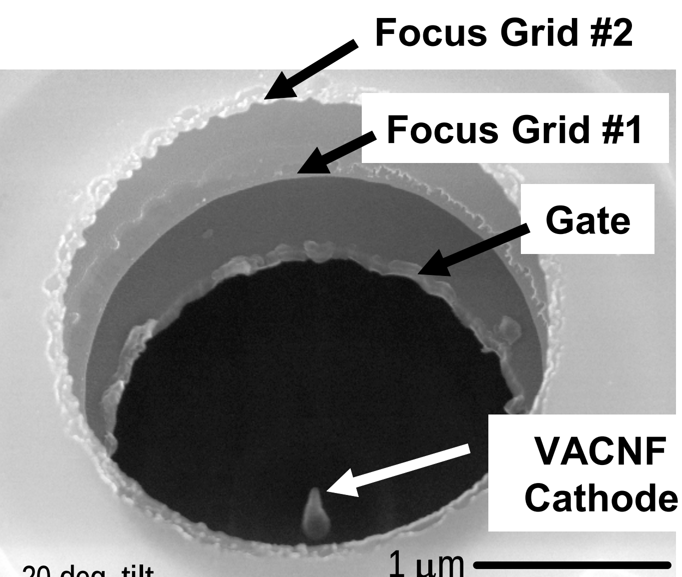
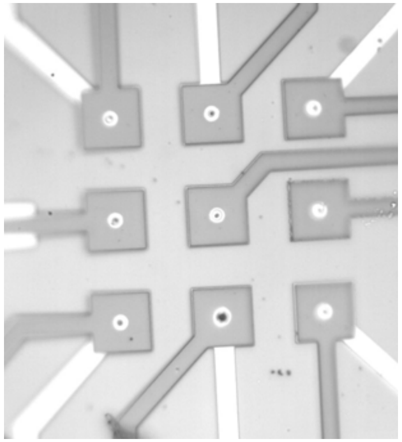
Massively Paralleled Electron Beam Lithography System

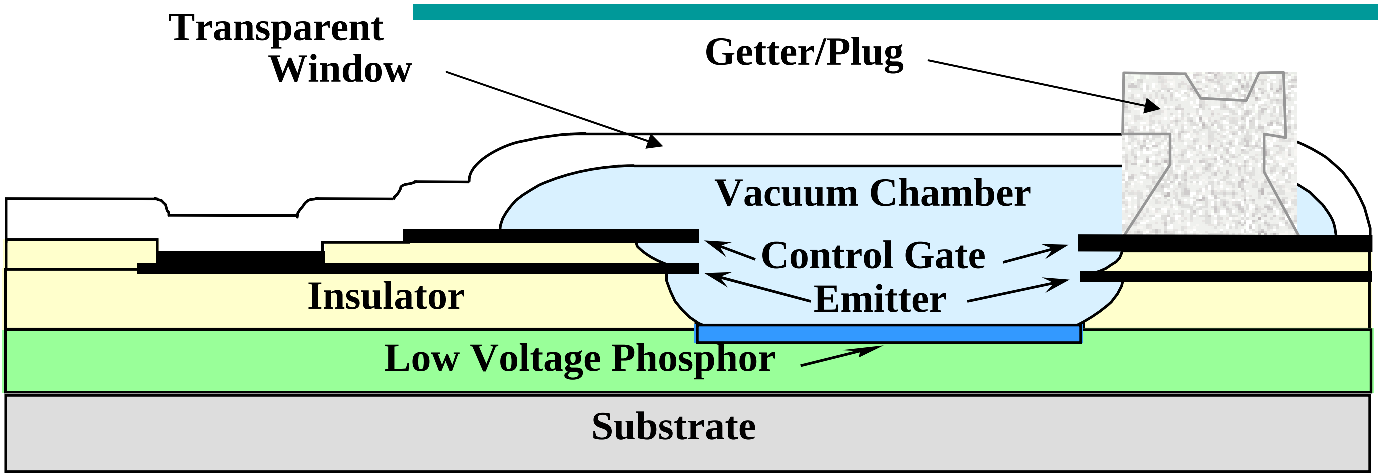






DEAL 3x3 FE array (100 µm spacing)

Integrated Phosphor - FED (IPFED)



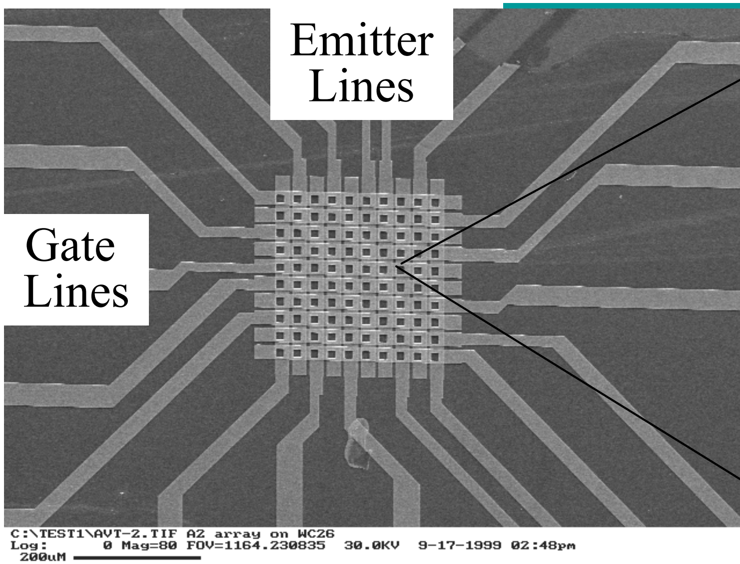
Device Properties

- Lateral emitter
- Micro-encapsulated pixels
- Thin film oxide phosphors
- Monolithic (single substrate)
- CMOS compatible

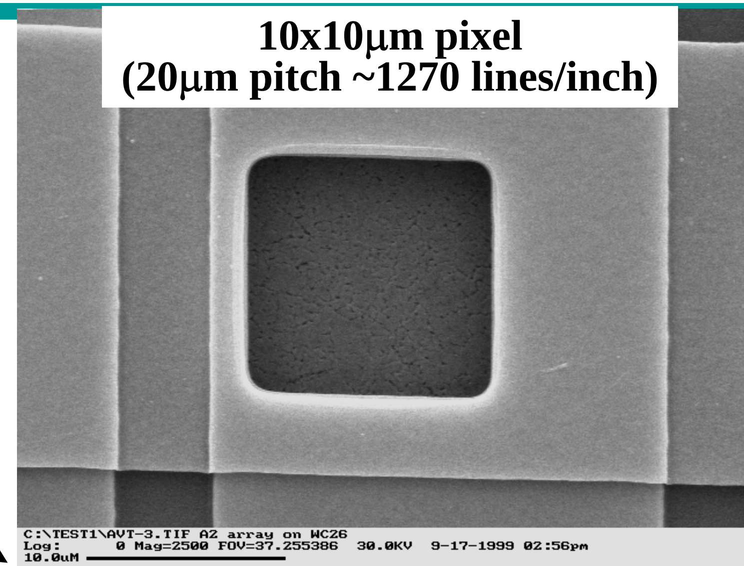
Process Steps

- Lithography (11 levels) (g-line → i-line)
- Materials Deposition
  - Sputter deposition (4)
  - Low pressure CVD (2)
  - Thermal evaporation (1)
  - Ion implantation (2)
- Etching
  - Reactive Ion Etch (10)
  - Wet Etching (1)

10x10 Prototype Development

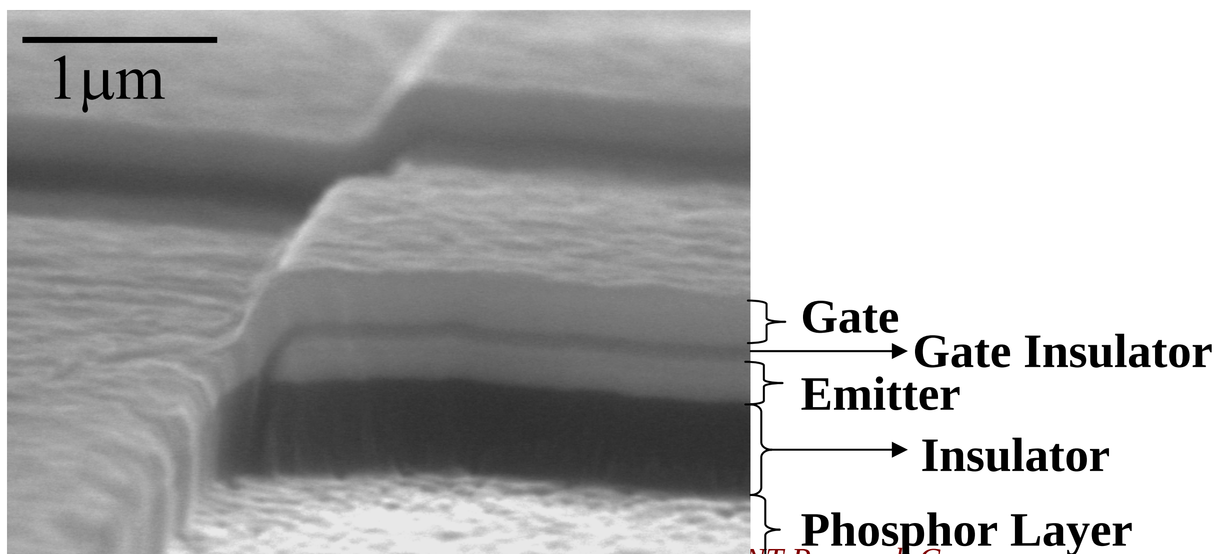


200µm

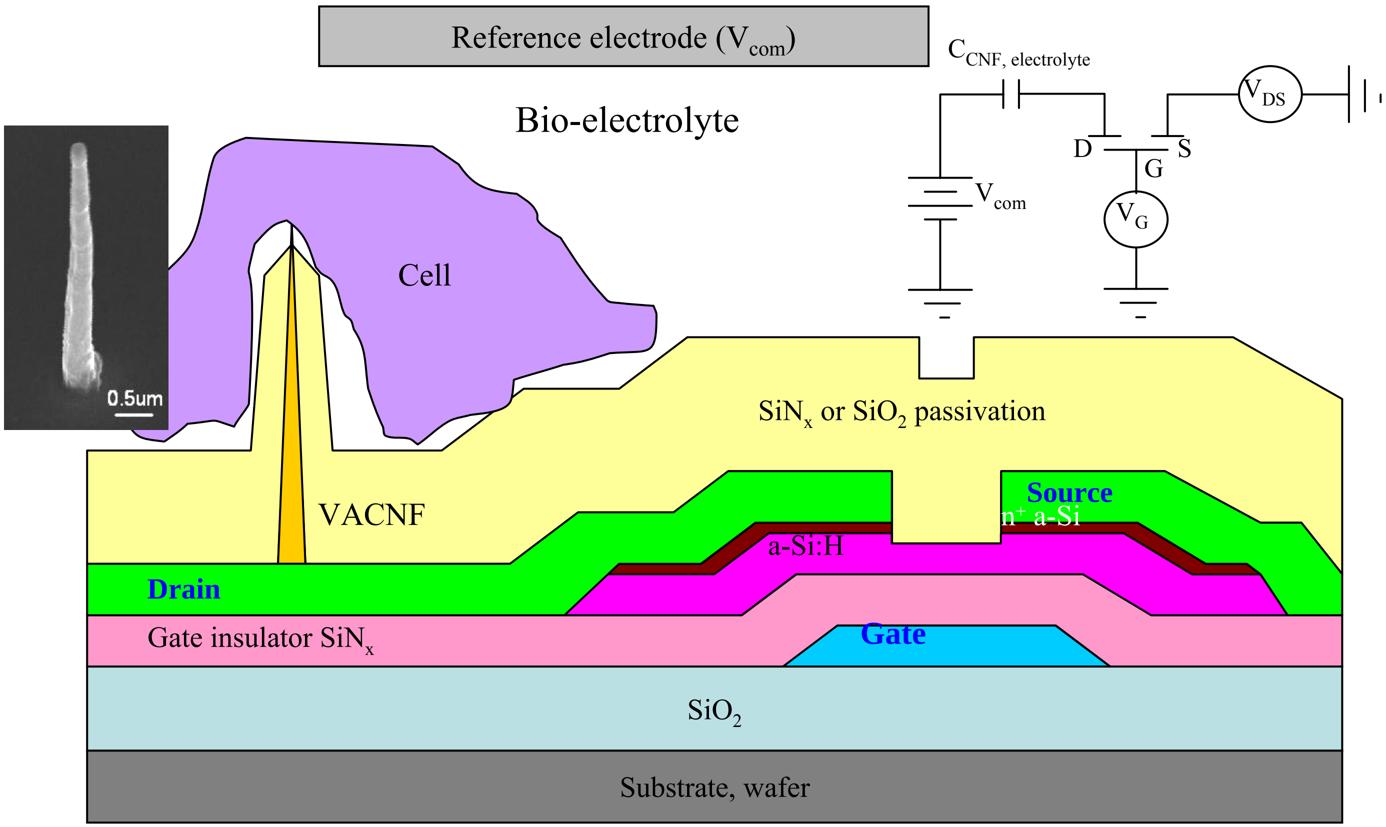


10µm

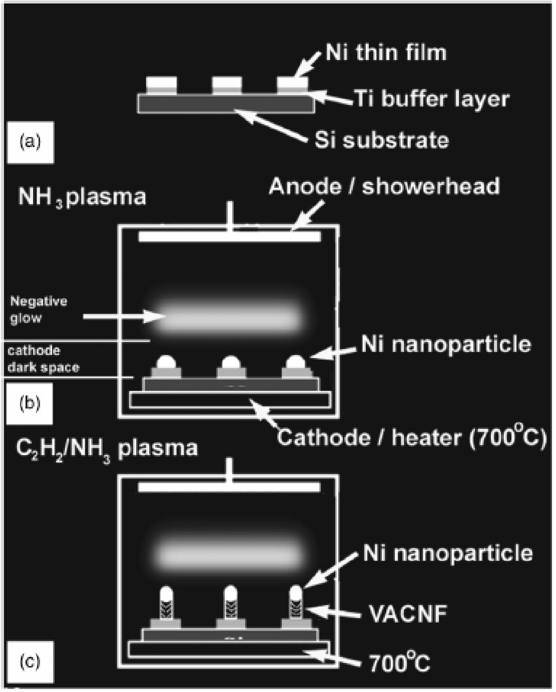
IPFED
Cross-Section



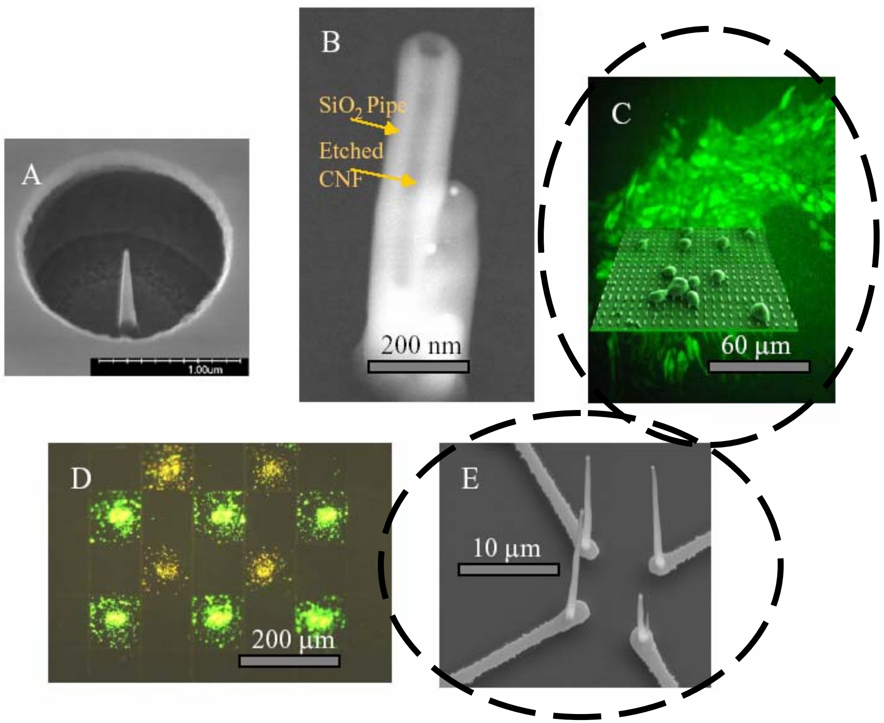
Active Matrix Thin Film Transistors for Biological Application



Vertically aligned carbon nanofibers (VACNFs)



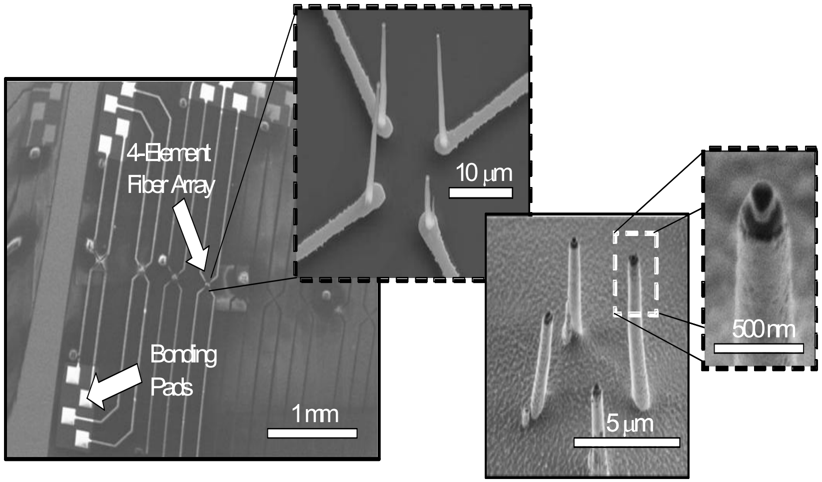
VACNF growth process in DC-PECVD
(a) Catalyst (Ni) deposition,
(b) Catalyst pretreatment/nanoparticle formation
(c) Growth of carbon nanofibers.

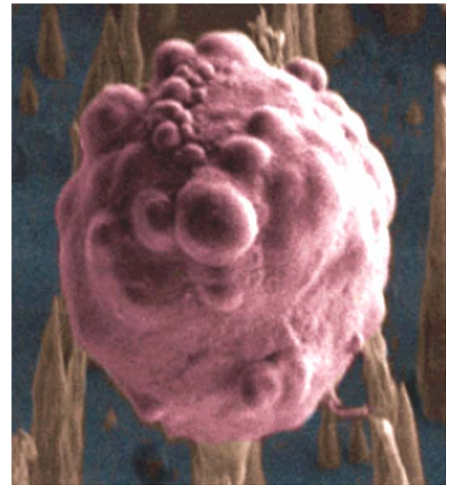


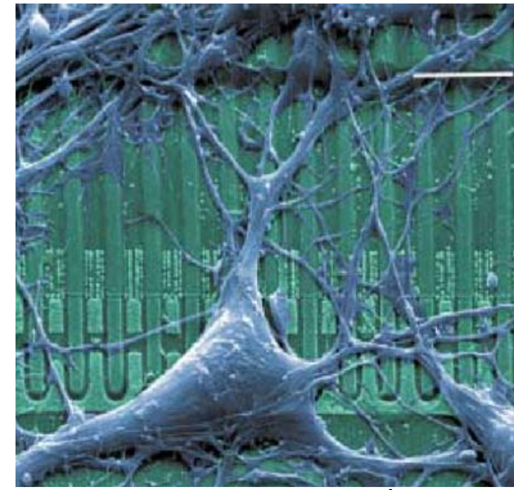
Applications of VACNF
(A) Self aligned field emission source
(B) Electrically addressed partial nanopipe
(C) Massively parallel needlelike arrays for gene delivery
(D) Vertical membranes (via nanofiber crowding) on microfluidic platforms
(E) Individually addressable electrochemical probe arrays.

VACNF intracellular/extracellular arrays for cell probing

Vertical-aligned carbon nanofiber array for cell probing (passively addressed)







P. Fromherz et al.

Intracellular probing into live cells

Extracellular probing

nerve cell from rat brain on a chip

- Electrically addressed individual nanofibers enable probing and manipulation of live cells.
- Deficiencies: limited probe density, can not simultaneously stimulate and record due to passive driving scheme.

T.E. McKnight, A. V. Melechko, M. L. Simpson, S. I. Jun, P. D. Rack, *et al.*, *Smart Med. and Biomed., Sens. Tech. II*, p128 (2004)

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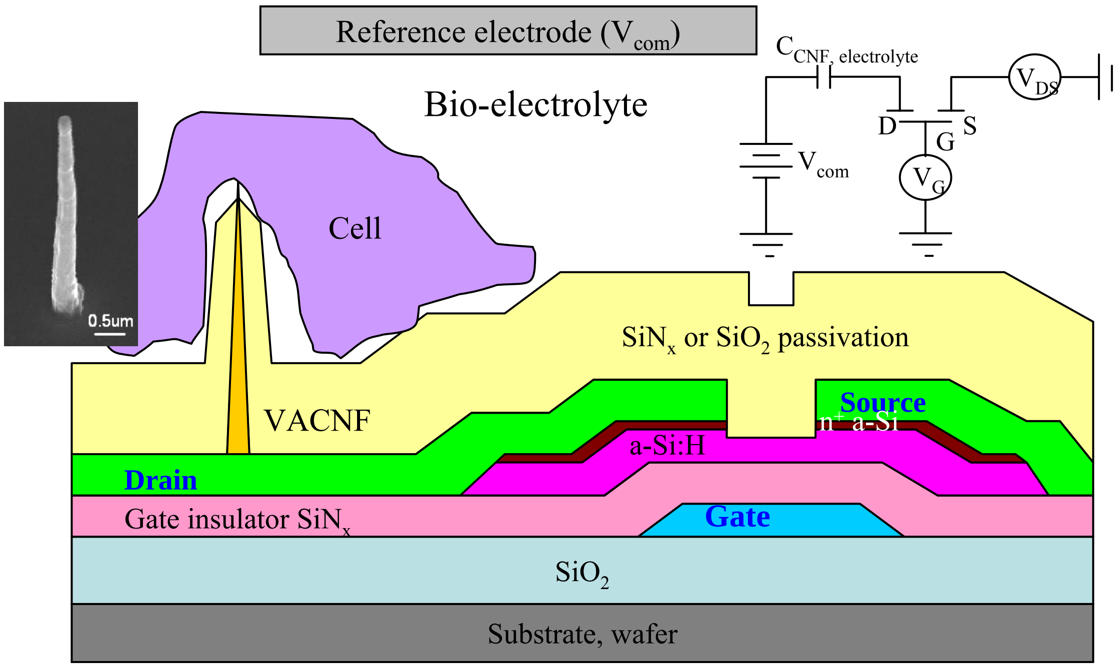
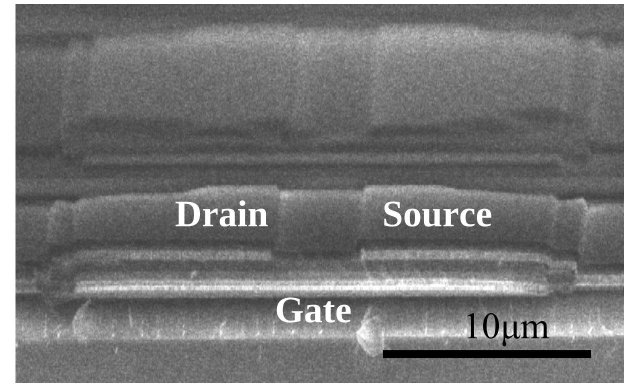
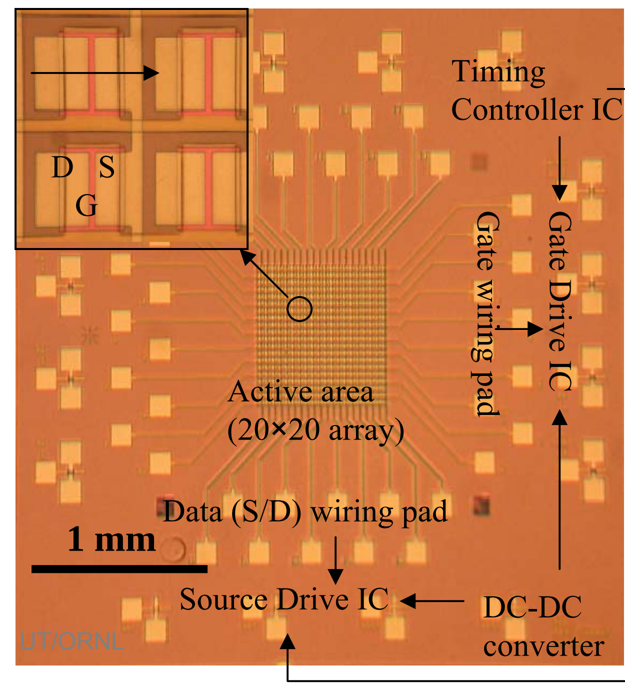
Goal: Integrate TFT array with VACNF for intracellular probing device

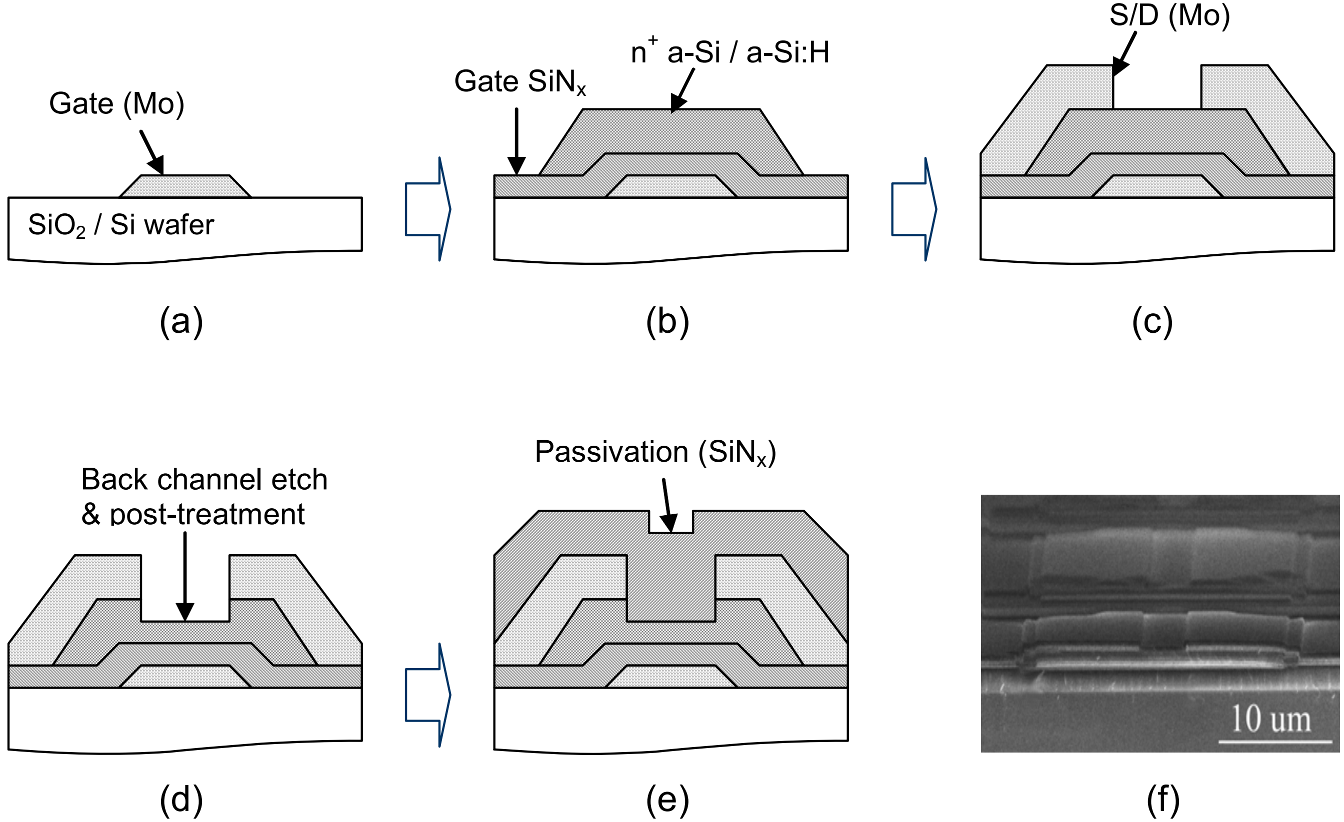






- Inverted-staggered back-channel etched (BCE) structure
- 20 x 20 array (400 electrodes), 50μm pitches
- High temperature compatible materials for VACNF growth ~700°C

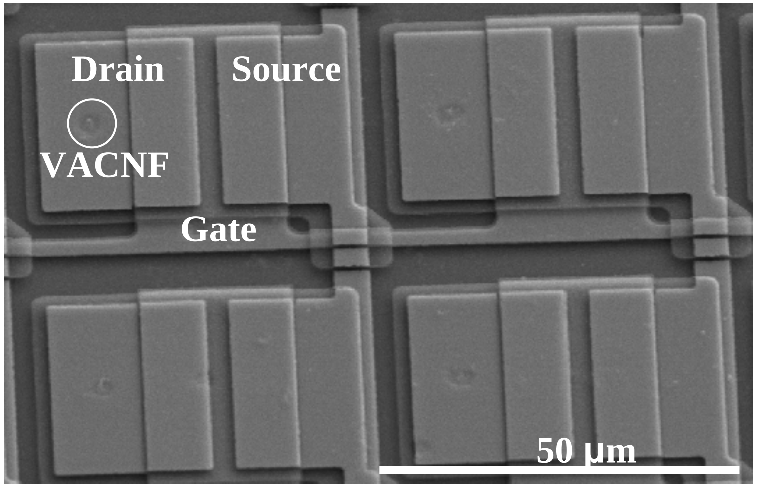
TFT fabrication; BCE process

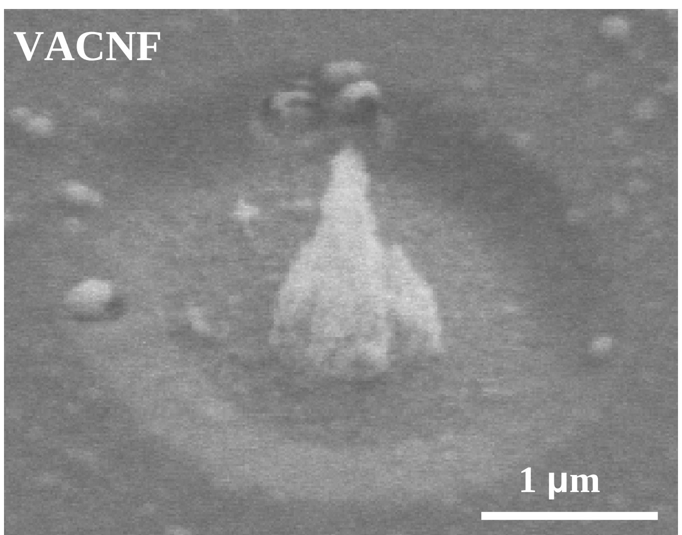


- Process sequence of TFT fabrication with back channel etch structure. (a) Gate electrode (Cr 250 nm), (b) active layers (gate SiN_x 300 nm, a-Si:H 200 nm, n^+ a-Si 50 nm), (c) source-drain electrode (Cr 300 nm), (d) back channel etch and post-treatment, (e) passivation (SiN_x 350 nm), (f) cross-sectional SEM image of inverted-staggered BCE-TFT.

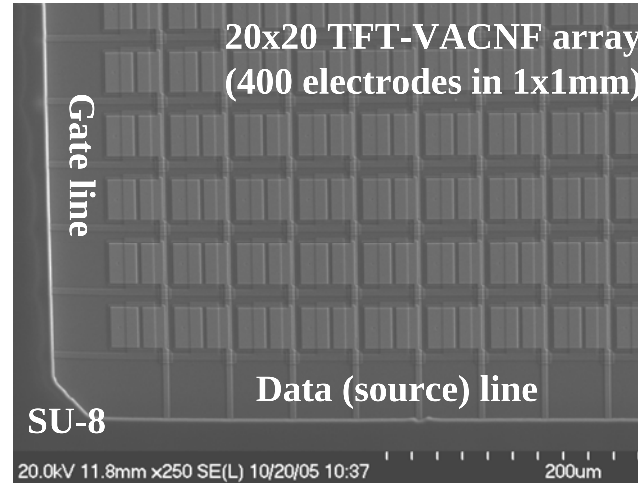
SEM images of TFT arrays

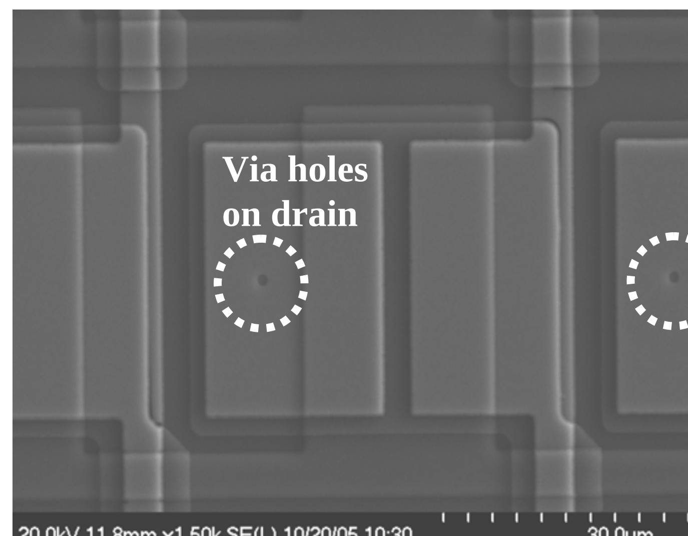
Intracellular probing TFT Array



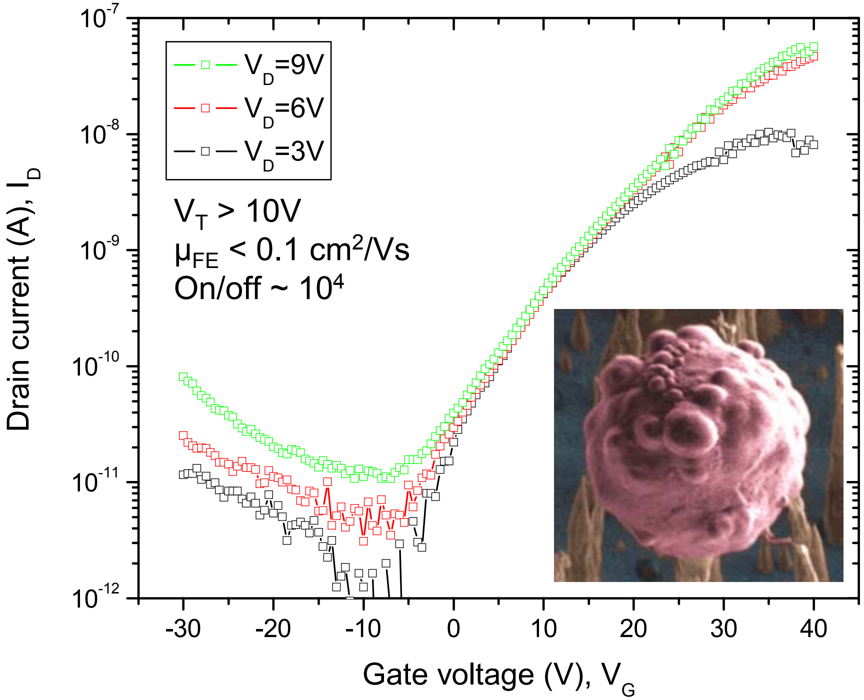


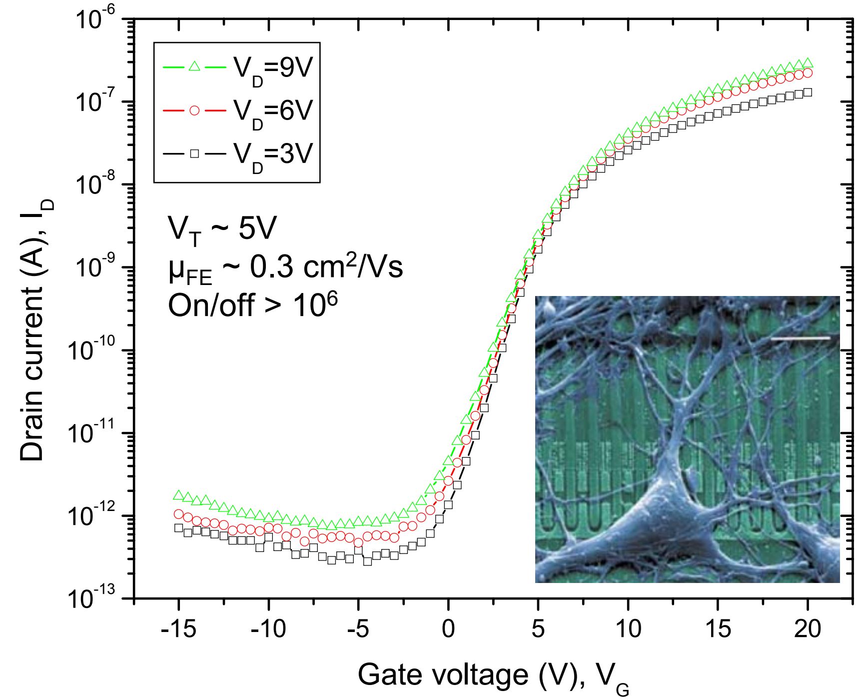
Extracellular probing TFT Array





Intra/extracellular TFT Device Characteristics II





- **Intracellular probing with VACNF**
- Unbiased sputter deposition
- Likely has more defects in films and consequently worse TFT device characteristics

- **Extracellular probing with via hole**
- Biased sputter deposition
- Improved electrical properties of TFT versus unbiased thin films
  - Lower leakage
  - higher transfer slope

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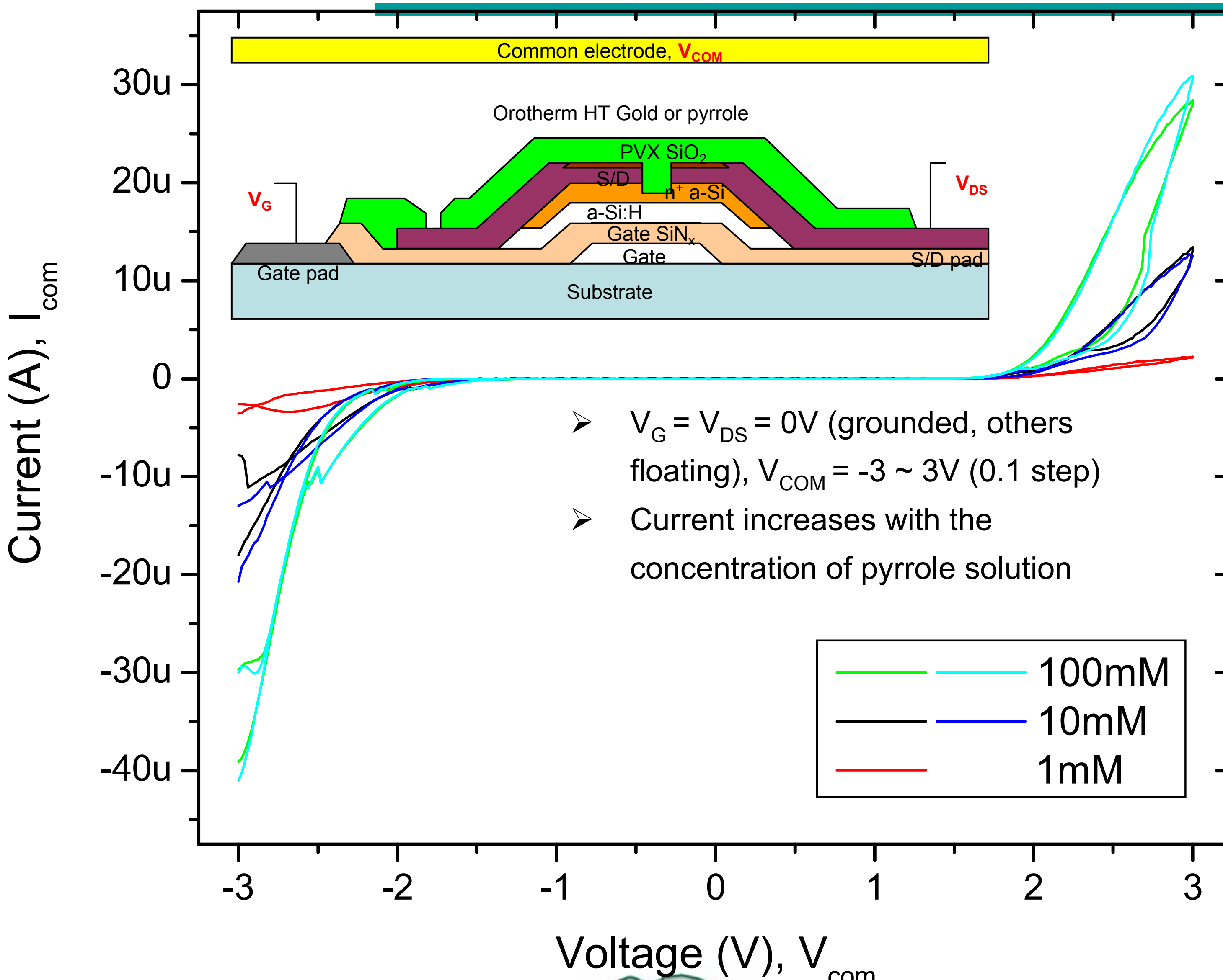
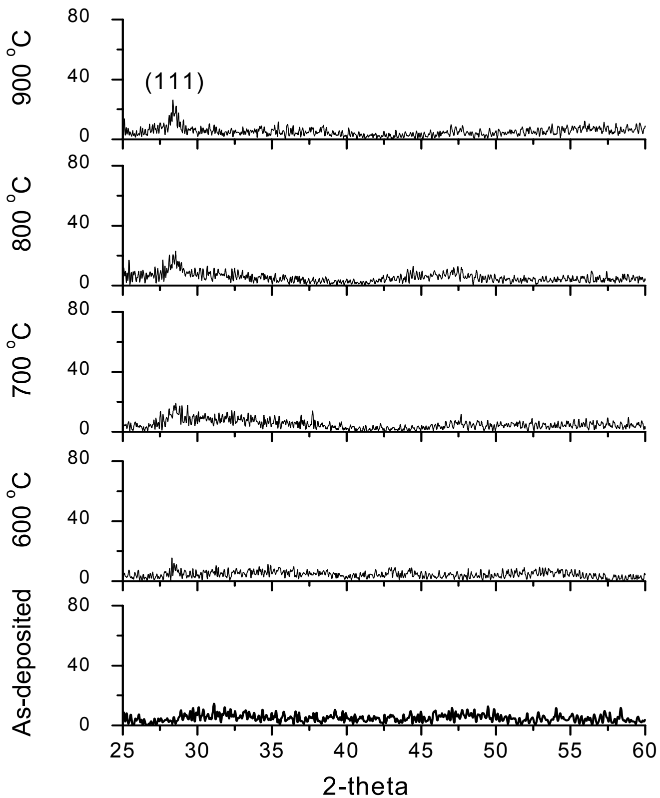
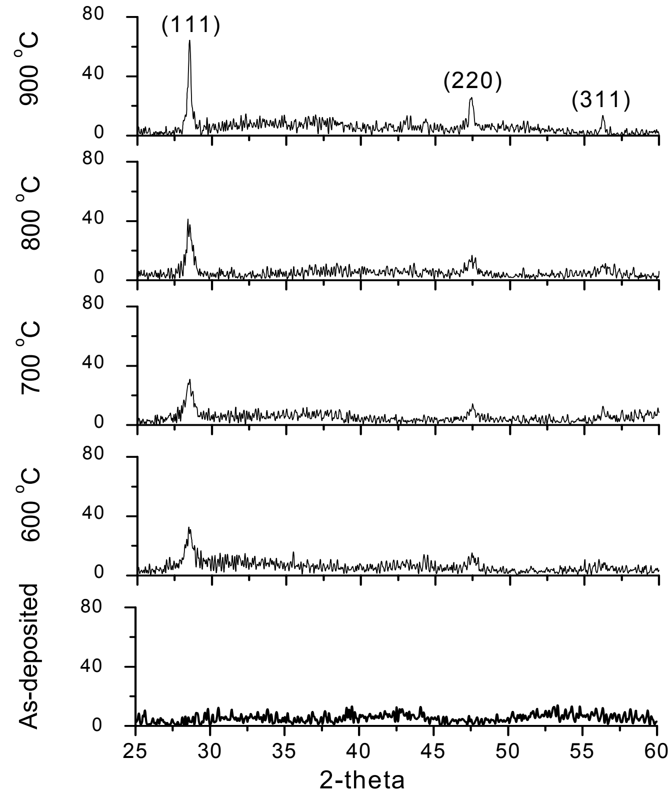
Electrochemistry with grounded V_G, V_{DS} (Extracellular)



Crystallization of sputter deposited a-Si



Unbiased a-Si annealing



30W biased a-Si annealing

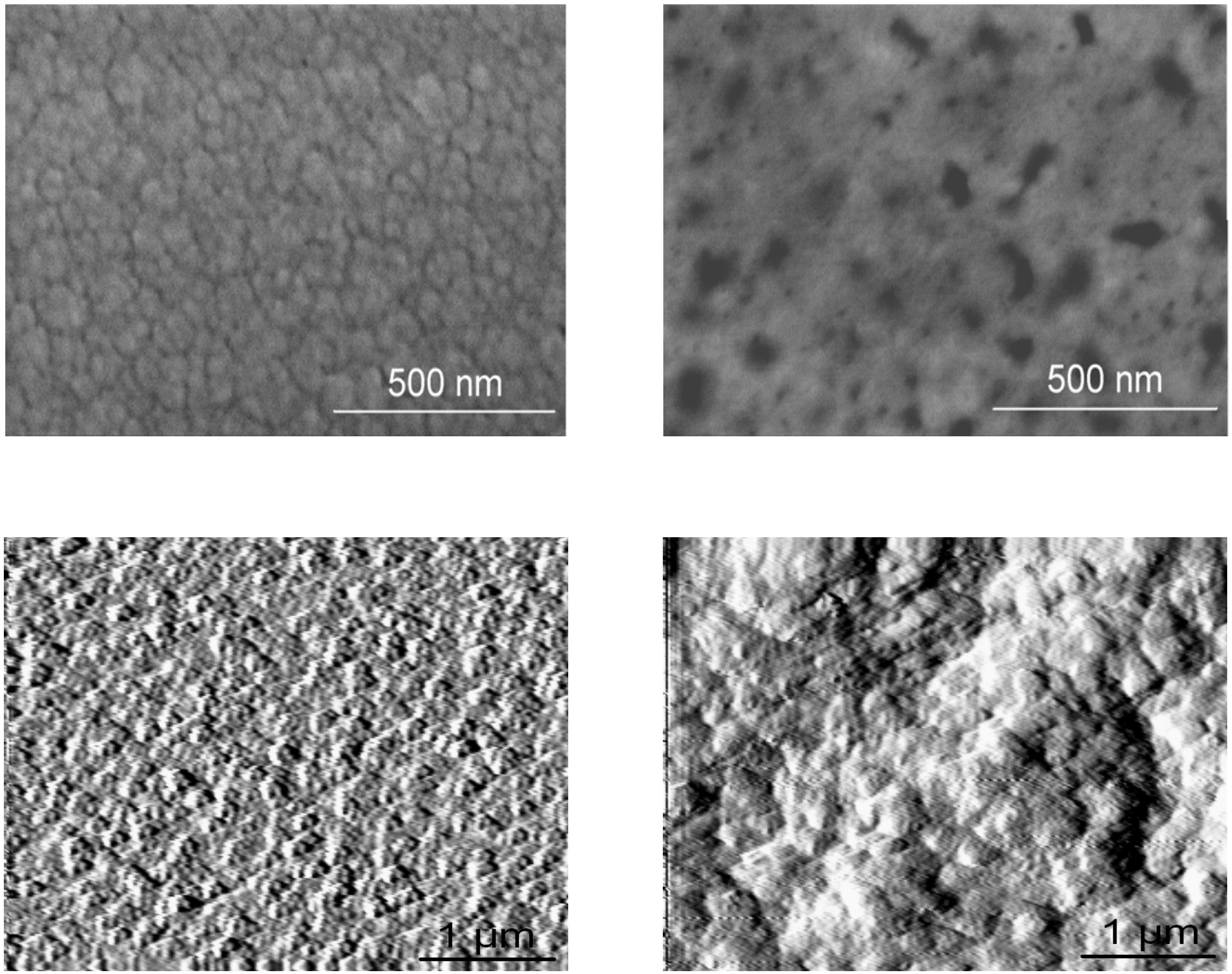
- During biased sputtering ion enhanced nucleation occurs which enhances the growth velocity during the post-deposition anneal → large grain and high crystallinity resulted.

a-Si:H recrystallization: Microstructure properties

Unbiased a-Si annealed at 900°C | **30W biased a-Si annealed at 900°C**

SEM

AFM



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- DEAL Device
  - DARPA Advanced Lithography Program
- Field Emission Array
  - AVT
- TFT array
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  - DARPA Advanced Lithography Program