Direct-current substrate bias effects on amorphous silicon sputter-deposited films for thin film transistor fabrication

Seung-Ik Jun[a)] and Philip D. Rack
Department of Materials Science and Engineering, The University of Tennessee, Knoxville, Tennessee 37996-2200

Timothy E. McKnight, Anatoli V. Melechko, and Michael L. Simpson
Molecular Scale Engineering and Nanoscale Technologies Research Group, Oak Ridge National Laboratory, Oak Ridge, Tennessee 37831

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The effect that direct current (dc) substrate bias has on radio frequency-sputter-deposited amorphous silicon (*a*-Si) films has been investigated. The substrate bias produces a denser *a*-Si film with fewer defects compared to unbiased films. The reduced number of defects results in a higher resistivity because defect-mediated conduction paths are reduced. Thin film transistors (TFTs) that were completely sputter deposited were fabricated and characterized. The TFT with the biased *a*-Si film showed lower leakage (off-state) current, higher on/off current ratio, and higher transconductance (field effect mobility) than the TFT with the unbiased *a*-Si film. © *2005 American Institute of Physics*. [DOI: 10.1063/1.2061860]

Amorphous silicon (*a*-Si) sputter deposition has been studied for the semiconducting layer of thin film transistors (TFTs) and solar cells.[1] Sputter deposition is particularly attractive for low temperature large area fabrication processes on transparent, flexible, and plastic substrates.[2,3] Sputtered *a*-Si films, however, typically have high trap densities which result in high off-state current when driving microelectronic devices.[4] For this reason, reasonable quality devices have not been demonstrated for sputter-deposited *a*-Si films. Liang, Maley, and Abelson have studied the electrical and microstructural properties of sputter-deposited *a*-Si at $\sim 350\ ^{\circ}C$.[4] In spite of having low defect densities compared to other research results, the films were deposited at even higher temperatures for flexible display applications. To achieve a low temperature deposition process and high device performance, a polycrystalline silicon technology has been developed by annealing sputtered *a*-Si films.[5] In this study, *a*-Si films were initially deposited on flexible substrates by rf magnetron sputtering at low temperatures (as low as room temperature), and then, the *a*-Si films were crystallized by excimer laser annealing. The flexible substrate is not thermally degraded since the excimer laser anneals only the top surface of the *a*-Si films. Even though the quality of the films is high, the excimer laser anneal process is complex and costly. Consequently, it is desirable to obtain high quality *a*-Si thin films without any posttreatment, and low temperature sputter deposition is a logical candidate.

It is well known that direct current (dc) substrate bias makes thin films denser and can reduce defects, which can have a pronounced effect on the electrical properties of thin films. That is, thin films can be densified, and thus have a void-free microstructure even when deposited at room temperature by applying a substrate bias. We recently studied the effects of substrate bias on rf-sputter-deposited MoW[6] electrodes and SiO_2[7] insulators. In this work, we evaluated the electrical properties of rf-sputter-deposited *a*-Si films with a substrate bias to show the effect of substrate bias on the electrical properties of *a*-Si films. Finally, to verify the effect of substrate bias, thin film transistors were fabricated with sputter-deposited *a*-Si with and without a substrate bias and their electrical characteristics were compared.

An AJA ATC2000 rf magnetron sputtering system, equipped with four magnetron sources and a heated and/or dc biased substrate holder, was utilized for the *a*-Si thin film deposition (Fig. 1). The base pressure before the sputter deposition was below 5.0×10^{-5} Pa and the process pressure was 0.4 Pa with a mass flow rate of argon–hydrogen (5% H_2) fixed at 25 sccm/min. The Si sputtering target has a 50 mm diameter and a 6 mm thickness. The film thickness was measured using a reflectometer (Filmeterics F20/40, Advanced Thin Film Measurement System). The electrical properties were measured using a HP 4156A, Precision Semiconductor Parameter Analyzer. All reported property values are an average of ten measurements for each sample.

Figure 2 shows the schematic diagram of an inverted-staggered back channel etch (BCE) TFT fabrication process.

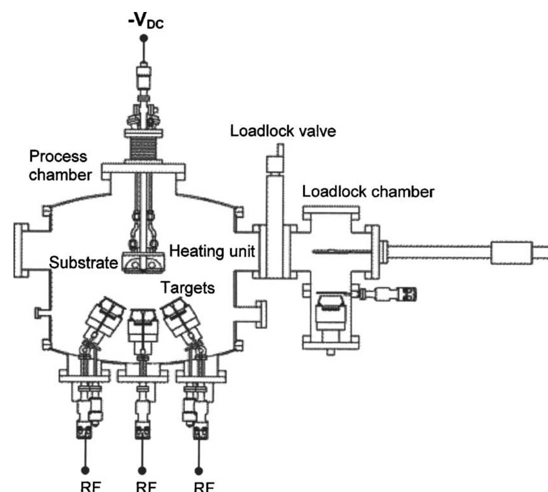

FIG. 1. Schematic diagram of an AJA ATC2000 rf magnetron sputtering system equipped with dc substrate bias supply

[a)]Author to whom correspondence should be addressed; electronic mail: sjun3@utk.edu

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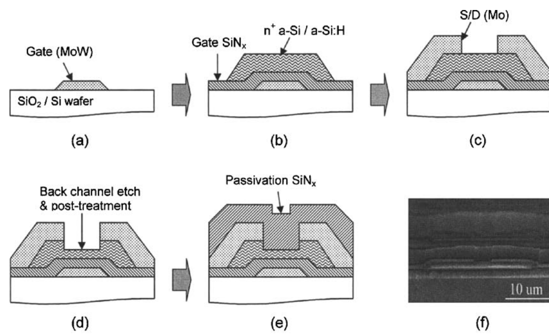
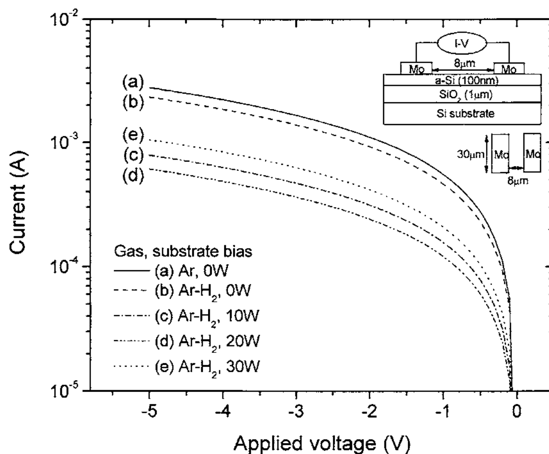


FIG. 2. Schematic diagram of inverted-staggered back channel etch (BCE) TFT fabrication process: (a) gate electrode (MoW), (b) active layer (gate SiN_x, *a*-Si, n^+ *a*-Si), (c) source-drain electrode (Mo), (d) back channel etch (BCE), (e) passivation (SiN_x), (f) cross-sectional scanning electron microscopy image of one transistor element in a 20×20 TFT array.

The process sequence is gate electrode deposition and pattern, oxide deposition, active layer deposition and pattern, source-drain electrode deposition and pattern, back channel etch, passivation deposition, and via hole pattern. All deposition processes are done by rf magnetron sputtering below 200 °C.

Figure 3(a) shows the current-voltage characteristics for *a*-Si films grown in Ar–H_2 as a function of applied substrate bias. To observe the effects of hydrogen in the sputtering gas, an additional zero-bias film was sputter deposited in pure Ar. The current of the *a*-Si film sputtered in an argon–hydrogen (5%) gas is lower than that of films sputtered in pure argon gas. It is well known that hydrogen atoms play an important role in *a*-Si:H films by compensating for defects such as dangling bond, vacancies, and dislocations.[8] These defects create energy levels near the conduction and valence bands which produce conduction paths for electrons and holes, respectively. This, in turn, effectively increases the current carried by the *a*-Si. Our previous study of the effects of substrate bias on sputter-deposited MoW films showed that biased films are denser and have fewer defects, which reduces the resistivity of the metal films.[6] In the case of *a*-Si, however, the thin films with fewer defects have a higher resistivity because, as mentioned previously, defects mediate conduction in semiconductors by providing energy states for carriers in an otherwise forbidden gap. In metal films, these defects scatter or impede electron conduction, resulting in higher resistivity.



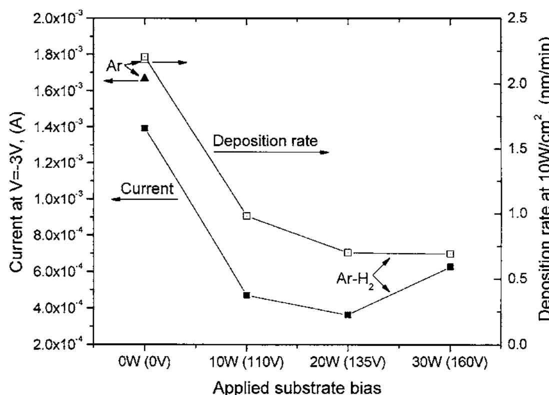


FIG. 3. (a) Current-voltage characteristics of sputtered *a*-Si thin films in Ar (zero bias) and Ar–H_2 as a function of dc substrate bias during sputter deposition, (b) current (at −3 V) and deposition rate changes as a function of substrate bias for films sputter deposited in Ar–H_2.

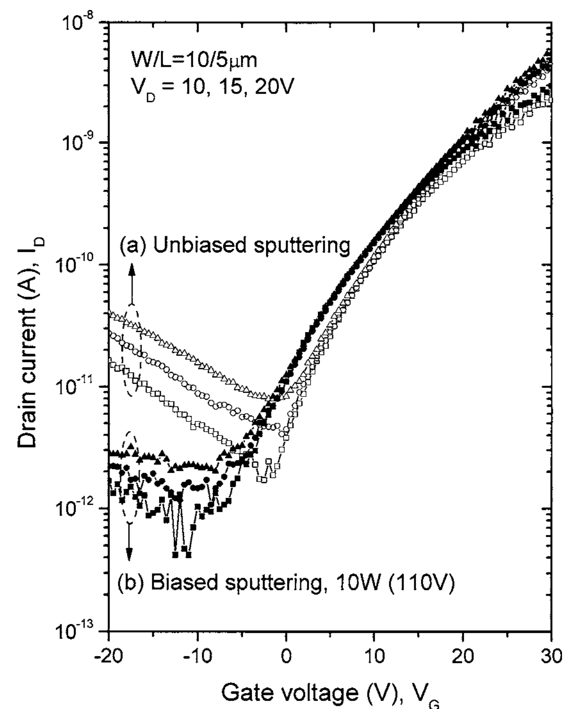


FIG. 4. Transfer characteristics of TFTs: (a) unbiased *a*-Si TFT, (b) dc biased *a*-Si TFT (both are characteristics before annealing).

Figure 3(b) shows the current at −3 V and the deposition rate for various sputtering conditions, gas mixture and substrate bias. The deposition rate decreases with increasing applied substrate bias. The lower deposition rate indicates that the films are denser, which is a result of energetic ion bombardment during growth. Figure 3(b) also demonstrates the correlation between the deposition rate (i.e., film density) and the resistivity of the films. The films with the lower deposition rate (denser films) correlate with the lower current at a −3 V bias.

To demonstrate advantages and possibilities of the substrate bias for microelectronics applications, 20×20 TFT arrays were fabricated. All films in the inverted-staggered BCE TFT structures were deposited by rf magnetron sputtering below 200 °C. For this study, we compared the electrical properties of TFTs with an *a*-Si active layer sputtered with

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(10 W, 110 V) and without substrate bias. As shown in Fig. 4, the on-state current of the biased *a*-Si TFT (b) is slightly higher than that of an unbiased *a*-Si TFT (a), which means that the biased *a*-Si TFT has a higher transconductance and field effect mobility. Second, the leakage (off-state) current of the biased *a*-Si is much lower than that of unbiased *a*-Si TFTs. The defect density in the films likely causes the high leakage current in unbiased *a*-Si TFTs. On the other hand, the biased a-Si TFT has an extremely low leakage current (less than a picoampere) because the biased *a*-Si is denser and has fewer defects.

In conclusion, we surveyed and verified the effects of substrate bias on *a*-Si sputtered films. Biased *a*-Si films exhibit lower leakage current and a lower deposition rate because they are denser films with fewer defects as a result of the energetic ion bombardment that occurs during bias sputtering. Additionally, we fabricated a fully sputter-deposited TFT with the biased *a*-Si that exhibit very low leakage and superior transconductance values relative to films deposited with no bias.

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[1]S. Bae, A. Kaan Kalkan, S. Cheng, and S. J. Fonash, J. Vac. Sci. Technol. A **16**, 1912 (1998).
[2]Y. Mishima, M. Takei, T. Uematsu, N. Matsumoto, T. Kakehi, U. Wakino, and M. Okabe, J. Appl. Phys. **78**, 217 (1995).
[3]C. S. McCormick, C. E. Weber, J. R. Abelson, G. A. Davis, R. E. Weiss, and V. Aebi, J. Vac. Sci. Technol. A **15**, 2770 (1997).
[4]Y. H. Liang, N. Maley, and J. R. Abelson, J. Appl. Phys. **75**, 3704 (1994).
[5]T. Voutsas, H. Nishiki, M. Atkinson, J. Hartzell, and Y. Nakata, Sharp Tech. J. **80**, 36 (2001).
[6]S. I. Jun, P. D. Rack, T. E. McKnight, A. V. Melechko, and M. L. Simpson, J. Appl. Phys. **97**, 054906 (2005).
[7]S. I. Jun, P. D. Rack, T. E. McKnight, A. V. Melechko, and M. L. Simpson, Electron. Lett. **41**, 59 (2005).
[8]Y. Kuo, J. Electrochem. Soc. **142**, 2486 (1995).

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